IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	09/905,218	Filing Date:	July 13, 2001
Confirmation No.:	4479		
First Named Inventor:	Alexander J. Berger		
Assignee:	Tru-Si Technologies, Inc.		
Examiner:	Krizek, Janice Lee	Art Unit:	3652
Attorney Docket No.:	M-11882 US		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF SAM KAO
UNDER 37 CFR 1.132

1. (a) My name is Sam Kao. I am the Director of Applications Development at Tru-Si Technologies, Inc. of Sunnyvale, California. Tru-Si Technologies, Inc. designs and manufactures semiconductor processing equipment including plasma etchers and wafer holders. Tru-Si Technologies also develops semiconductor integrated circuit manufacturing processes for its customers. More information about Tru-Si Technologies can be obtained from the company web site at www.trusi.com.

(b) I hold a Ph.D. degree in Fluid Mechanics and Hear Transfer from the University of Michigan, Ann Arbor.

(c) I have been doing engineering work at Tru-Si Technologies, Inc. from August of 1999 until the present time.

(d) From August of 1999 until August of 2001, I was working at Tru-Si Technologies on a plasma etcher and wafer holder design. I was part of an engineering team that designed plasma etchers and wafer holders. My position was initially a Senior

Mechanical Engineer. In January of 2001, I became a Senior Manager of Applications Development. In August of 2001, I became a Director of Applications Development.

(e) From August of 2001 until the present time, I have been developing semiconductor integrated circuit manufacturing processes at Tru-Si Technologies. I have been using wafer holders during this time.

(f) I am named as an inventor in U.S. patent no. 6,749,764 (issued June 15, 2004), U.S. patent no. 6,427,991 (issued August 6, 2002) and U.S. patent application no. 09/877,366 (published December 12, 2002 as 2002/0185230), all of which relate to wafer holder design and/or use.

2. I have reviewed the Japanese patent document JP 61-254437 (inventor: Matsuyama) and its English translation which was filed in the present patent application on July 28, 2004. I do not believe that Matsuyama discloses a rotation of wafer chuck surface 11 (Fig. 2) relative to the top portion of the chuck.

3. In particular, Matsuyama's reference to the wafer rotation on page 4, line 15 of the English translation does not imply that the bottom surface 11 rotates relative to the top portion of the chuck. Matsuyama could instead be referring to the rotation of the whole chuck. Matsuyama states on page 3, lines 1-3 that in a prior art Bernoulli chuck, the wafer was in a "floating state", was "not reliably chucked", and hence could not be rotated. Therefore, I believe the rotation statement on page 4, line 15 means that the wafer can be rotated due to its engagement with the surface 11 as opposed to the floating state in the prior art chuck. Note the English translation, page 3, lines 42-43 stating that in the chuck of Fig. 2, the wafer is "chucked to the chucking surface". Matsuyama does not teach or suggest that the surface 11 could rotate relative to the top portion of the chuck.

4. Further, Matsuyama's Fig. 2 shows an orifice 13, described in the English translation on page 3, lines 35-43. Orifice 13 is a passage between the chuck's top and bottom portions. The plan view of Fig. 1(b) shows multiple orifices 13. The orifices are spaced from each other. Between the orifices, the chuck's bottom portion could rigidly connect to the top portion, preventing any relative movement between the surface 11 and the

top portion. Whether or not there is a rigid connection or relative movement, Matsuyama does not teach or suggest that the surface 11 can rotate relative to the top portion.

5. I certify that all statements made herein of my knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the present application, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

Name: Sam Kao

Signature:  Date: 11/24, 2004